rd

rs2

opcode

rs1

Forward

unit

STAGE 2

Instruction Decode

**Function4**

**(4-bits)**

STAGE 3

Execution

Mem

Ex

WB

STAGE 6

WriteBack

STAGE 5

Memory

STAGE 4

Execution

**Control unit**

WB

WB

Mem

STAGE 1

Instruction Fetch

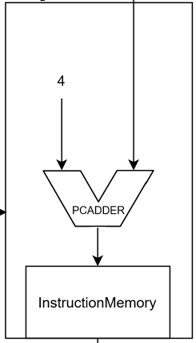
WB

**Opcode**

**(3-bits)**

INSTRUCTION SEPERATION

**IF/ID BUFFER**



Result

rd(3-bits)

Result

rd

imm

rs1

rs2

rd

**M**

**U**

**X**

**1**

**M**

**U**

**X**

**2**

rd



writeback

rd

writeback

data

(rs2) 32-bits

rs2

rd

rs2

Result

**Mem/WB BUFFER**

rs2

Result

Result’

rs2

rs1(3-bits)

rs2(3-bits)

rs1

rs1

**EX2/Mem BUFFER**

**32-BITS**

**EX1/EX2 BUFFER**

Multiplication

division

Fixing the

exponents

2’s compliment

Addition

DataMemory

1

& INT

**PC**

Register

file

(rs1) 32-bits

**ID/EX BUFFER**

Ex

Mem

rd(3-bits)